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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,220	02/13/2002	Minoru Tajima	027260-514	4808

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Platon N. Mandros
BURNS, DOANE, SWECKER & MATHIS, L.L.P.
P.O. Box 1404
Alexandria, VA 22313-1404

EXAMINER	
GLENN, KIMBERLY E	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 05/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/073,220	TAJIMA, MINORU	
	Examiner	Art Unit	
	Kimberly E Glenn	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☒ Claim(s) *19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☑ All b)☐ Some * c)☐ None of:

1.☑ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 7-9 and 16-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regard to claims 7 and 16, applicant disclose a microstrip line including a ground conductor formed on another the surface of the dielectric substrate. Is applicant replacing the conductive line disclose in claim 1, with the microstrip line or is applicant adding a microstrip line to the circuit? With regards to claims 8,9,17 and 18, the same question is asked. Is applicant replacing the conductive line with coplanar line including one or two ground conductors or is applicant adding a coplanar line to the circuit.

Drawings

In light of the 35 USC 112 rejection, if applicant is adding a microstrip line or coplanar line. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the microstrip line or coplanar line a long with the conductive line disclosed in claim 1 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

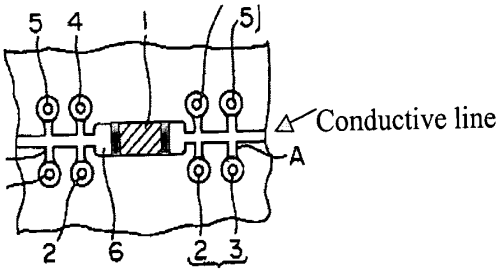
Claim Rejections - 35 USC § 102

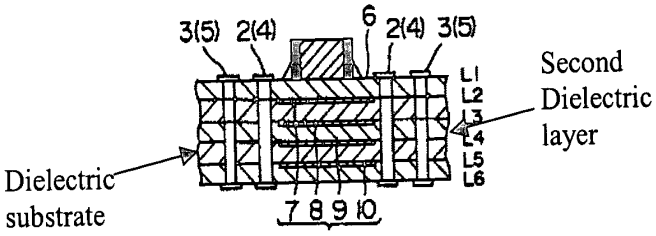
The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Sugawara et al US Patent 5,636,099 (of record).

Sugawara discloses a conductive line disposed on one surface of a dielectric substrate; an interdigital capacitor 9 forming apart of said conductive line; and a chip capacitor 1 that is disposed so that said interdigital capacitor is sandwiched between said chip capacitor 1 and said dielectric substrate. The conductive line is connected to interdigital capacitor by a hole 4. Sugawara further disclose a second dielectric layer (insulator) over the interdigital capacitor.





Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugawara et al US Patent 5,636,099 (of record).

Sugawara et al teach cirucit comprising a conductive line disposed on one surface of a dielectric substrate; an interdigital capacitor 9 forming apart of said conductive line; and a chip capacitor 1 that is disposed so that said interdigital capacitor is sandwiched between said chip capacitor 1 and said dielectric substrate.

Thus Sugawara et al is shown to teach all the limitation with the exceptions of the following:

- Connectors on both ends of said conductive line.
- The conductive line, interdigital capacitor, and chip capacitor have substantially equal widths.
- The chip capacitor having a width greater than that of the conductive line.
- The interdigital capacitor having a width greater than that of the conductive line.
- The insulator being a resist film.
- The conductive line is a microstrip line including a ground conductor formed on another surface of said dielectric substrate.
- The conductive line is coplanar line including a ground conductor formed on the surface of said dielectric substrate.

- The conductive line is a grounded coplanar line including two ground conductors respectively formed on the surface and another surface of said dielectric substrate.

One skilled in the art at the time of the invention would have found it obvious to provide the circuit of Sugawara et al with connectors on both ends of the conductive line in order to provide a means to connect the circuit with other components.

One skilled in the art, at the time of the invention, would have found an obvious matter of design choice to have the conductive line, interdigital capacitor and the chip capacitor have the same width, the chip capacitor or the interdigital capacitor having a width greater than the conductive line, since such a modification would involve a mere change in the size (i.e. width) of the components. A change in size (width) is generally recognized as being within the level of ordinary skill in the art.

One skilled in the art, at the time of the invention, would have found it obvious to replace the general conductive line of Sugawara et al with a microstrip line or a coplanar line having one or two ground planes, since examiner takes notice of the equivalence of the general conductive line and the microstrip or coplanar lines for their use in the transmission art and the selection of any of these known equivalents to provide a transmission means would be within the level of ordinary skill in the art.

One skilled in the art, at the time of the invention, would have found it obvious to replace second dielectric layer of Sugawara et al with resist film, since examiner takes notice of the equivalence of the general second dielectric layer and resist film for their use in the transmission art and the selection of any of these known equivalents to provide a insulating means would be within the level of ordinary skill in the art.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lau US Patent 5, 896,417 in view of Sugawara et al US Patent, 5,636,099(of record).

The primary reference, Lau, teaches a communication equipment comprising: a DC block capacitor, a first electric circuit 32R connected to an end of said DC block circuit (CR+ CR-); and a second electric circuit 42R connected to another end of said DC block circuit, said second electric circuit having a bias supply voltage different from that of said first electric circuit.(figure 5 and column 12 lines 55 through 66)

Thus, Lau is shown to teach all the limitations of the claims with the exceptions of the following:

- The dc blocking capacitor being comprised of a conductive line disposed on one surface of a dielectric substrate, an interdigital capacitor forming a part of said conductive line, and a chip capacitor that is disposed so that said interdigital capacitor is sandwiched between said chip capacitor and said dielectric substrate.
- Connectors on both ends of said conductive line.

- The conductive line, interdigital capacitor, and chip capacitor have substantially equal widths.
- The chip capacitor having a width greater than that of the conductive line.
- The interdigital capacitor having a width greater than that of the conductive line.
- The insulator being a resist film.
- The conductive line is a microstrip line including a ground conductor formed on another surface of said dielectric substrate.
- The conductive line is coplanar line including a ground conductor formed on the surface of said dielectric substrate.
- The conductive line is a grounded coplanar line including two ground conductors respectively formed on the surface and another surface of said dielectric substrate.

Sugawara et al shows that it is known in the art for a capacitor to be comprised of a conductive line, a dielectric substrate, interdigital capacitor and a chip capacitor. Refer to 35 USC 102 rejection for details of Sugawara et al reference.

One skilled in the art, at the time of the invention, would have found it obvious to replace the general capacitor of Lau with capacitor as taught in Sugawara et al, since examiner takes notice of the equivalence of the general capacitor and the capacitor of Sugawara for their use in the transmission art and the selection of any of these known equivalents to provide a capacitance means would be within the level of ordinary skill in the art.

One skilled in the art at the time of the invention would have found it obvious to provide the circuit of Sugawara et al with connectors on both ends of the conductive line in order to provide a means to connect the circuit with other components.

One skilled in the art, at the time of the invention, would have found an obvious matter of design choice to have the conductive line, interdigital capacitor and the chip capacitor have the same width, the chip capacitor or the interdigital capacitor having a width greater than the conductive line, since such a modification would involve a mere change in the size (i.e. width) of the components. A change in size (width) is generally recognized as being within the level of ordinary skill in the art.

One skilled in the art, at the time of the invention, would have found it obvious to replace the general conductive line of Sugawara et al with a microstrip line or a coplanar line having one or two ground planes, since examiner takes notice of the equivalence of the general conductive line and the microstrip or coplanar lines for their use in the transmission art and the selection of any of these known equivalents to provide a transmission means would be within the level of ordinary skill in the art.

One skilled in the art, at the time of the invention, would have found it obvious to replace second dielectric layer of Sugawara et al with resist film, since examiner takes notice of the equivalence of the general second dielectric layer and resist film for their use in the transmission art and the selection of any of these known equivalents to provide a insulating means would be within the level of ordinary skill in the art.

Allowable Subject Matter

Claims 19 and 20 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: With regards to claim 19, the prior art of record does not disclose or fairly teach the first electric circuit being a multiplexing circuit and the second electric circuit being a EA modulator that generates an intensity modulated optical signal. With regards to claim 20, the prior art of record does not disclose or fairly teach the first electric circuit being a photo diode with a preamplifier and the second circuit being a demultiplexer.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Mandai et al US Patent 5,384,434, Senqupta US Patent 6,556,102 and Martens et al US Patent 5,019,721.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly E Glenn whose telephone number is (703) 306-5942. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (703) 308-4909. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Kimberly E Glenn
Examiner
Art Unit 2817

keg
May 1, 2003

Robert Pascal
Supervisory Patent Examiner
Technology Center 2800